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U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

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INFORMATION DISCLOSURE STATEMENT		Docket Number: 10746/32	
Application Number 10/092,089	Filing Date March 5, 2002	Examiner Not Yet Assigned	Art Unit 2859
Title CLOCK/DATA RECOVERY CIRCUIT		Applicant(s) Keiji KISHINE et al	

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Address to:
Assistant Commissioner for Patents
Washington D.C. 20231

1. In accordance with the duty of disclosure under 37 C.F.R. § 1.56 and in conformance with the procedures of 37 C.F.R. §§ 1.97 and 1.98 and M.P.E.P. § 609, attorneys for Applicant hereby bring the references listed on the attached modified PTO Form No. 1449 to the attention of the Examiner. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

2. A copy of each patent, publication or other information listed on the modified PTO form 1449 is enclosed, except as otherwise indicated.

3. It is believed that no fees are due in connection with this Information Disclosure Statement. However, should any fees be due, the Commissioner is authorized to charge Deposit Account No. 11-0600 for such fees. A duplicate copy of this communication is enclosed for charging purposes.

Dated: 7/10/2002 By: _____

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO-1449 FORM	ATTY. DOCKET NO. 10746/32	U.S. SERIAL NO. 10/092,089
	APPLICANT KISHINE et al.	
	FILING DATE March 5, 2002	GROUP 2859

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	06252654	September 9, 1994	Japan			X	
	11055082	February 26, 1999	Japan			X	
	10126400	May 15, 1998	Japan			X	

* Copy of reference is not enclosed because reference is cited and described in Search Report (copy of reference provided by International Searching Authority).

OTHER DOCUMENTS

EXAMINER INITIAL		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
		Noboru Ishihara, Yukio Akazawa, "A Monolithic 156 Mb/s Clock and Data Recovery PLL Circuit Using the Sample-and-Hold Technique", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 29, NO. 12, DECEMBER 1994, pp. 1566-1571.
		D. Clawin, U. Langmann, "Multigigabit/second Silicon Decision Circuit", ISSCC 85, February 1985, pp.222-223.
		M. Wurzer, J. Bock, W. Zirwas, H. Knapp, F. Schumann, A. Felder, L. Treitinger, "40Gb/s Integrated Clock and Data Recovery Circuit in a Silicon Bipolar Technology", IEEE BCTM 8.1, Sep. 27-29, 1998.
		J. Savoj, B. Razavi, "A 10 Gb/s CMOS Clock and Data Recovery Circuit with Frequency Detection", ISSCC 2001, February 5, 2001.
		D. Clawin, U. Langmann, B.G. Bosch, "Silicon Bipolar Decision Circuit Handling Bit Rates up to 5Gbit/s", Journal of lightwave technology, Vol. LT-5, No. 3, March 1987, pp.348-354.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	